(c) Write short notes on the following :

(i) Transition and diffusion capacitance of p-n junction diode

(ii) Construction of a CRT.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3302 Roll No.

B. Tech.

(SEM. II) THEORY EXAMINATION 2011-12

ELECTRONICS ENGINEERING

Time : 3 Hours *Total Marks : 100*

Note : All sections are compulsory.

SECTION—A

1. All questions are compulsory. All questions carry equal marks : **(10×2=20)**

(a) Describe the difference between donor and acceptor impurities.

(b) What is voltage multiplier ?

(c) What is the ripple factor for full wave rectifier ?

(d) Derive the relation between α and β for BJT.

(e) Write down the stability factors for BJT amplifier.

(f) What is pinch-off condition in FET ?

(g) Draw the circuit of voltage summer using Op-amp and write the expression.

(h) What are MAXTERM and MINTERM ?

(i) What are Lissajous figures ?

(j) What are the necessary blocks in the multimeter for measuring AC voltage ?

(b) Justify the sentence 'the zener diodes are used as voltage regulators and limiters'.

Design the network of Figure 3 to maintain V_L at 12 V for a load variation (I_L) from 0 mA to 200 mA. That is, determine R_S and V_Z.

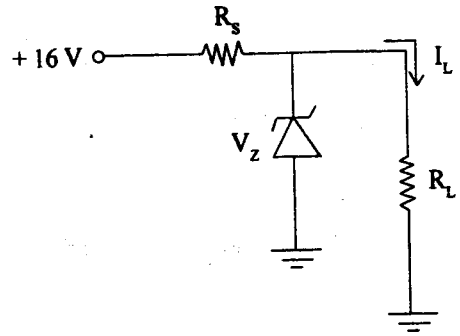

Figure 3

(c) For the network of Figure 4 :

(i) Calculate 5τ

(ii) Compare 5τ to half the period of the applied signal

(iii) Sketch v_0.

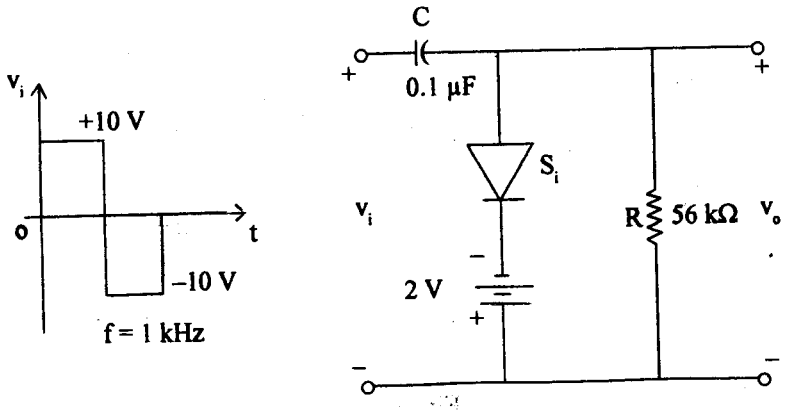

Figure 4

4. Attempt any **two** parts of the following. All questions carry equal marks :

(a) What do you mean by Limits of operation in BJT amplifier ? Also draw the input and output characteristics of a BJT in the common base configuration.

(b) Draw and solve the Voltage divider bias circuit of BJT by any one of the method.

(c) For the circuit shown in Figure 5 :

(i) Determine I_C

(ii) Prove stabilization factor $S(I_{CO}) = \dfrac{\beta + 1}{1 + \beta \dfrac{R_E}{R_E + R_B}}$.

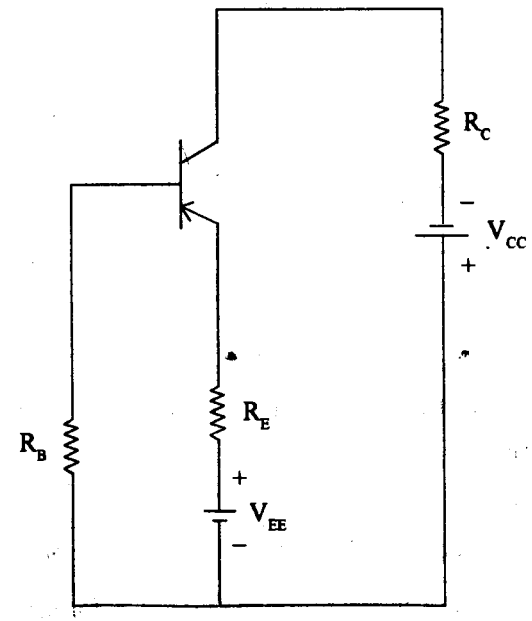

Figure 5

5. Attempt any **two** parts of the following. All questions carry equal marks :

(a) Draw and solve the self-bias configuration of JFET.

(b) Explain the construction and working of n-channel depletion type MOSFETs.

(c) The network of Figure 6 is not operating properly. What is the specific cause of its failure ?

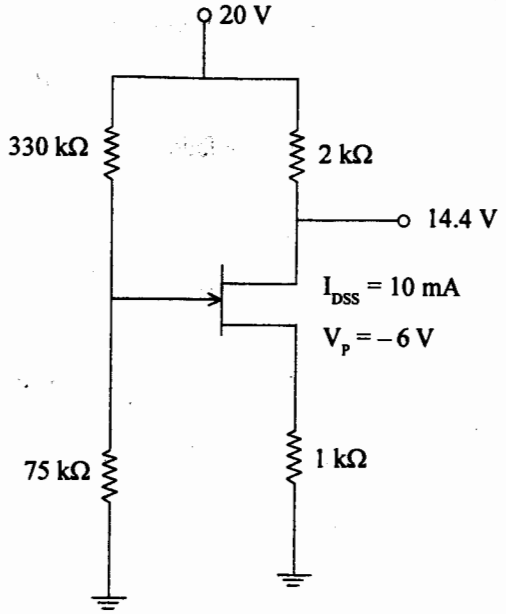

Figure 6

6. Attempt any **two** parts of the following. All questions carry equal marks :

(a) (i) Convert the following :

$(389)_{10} = (\ )_6$ $(FB27)_{16} = (\ )_8$ $(11001101)_2 = (\ )_{10}$

(ii) Convert the following into POS format :

$y(A, B, C, D) = (A + B + C) . (A + D)$

(b) (i) Design a circuit using only NOR gates for Boolean expression :

$Y = ABC' + BCD' + CD.$

(ii) Subtract by using r's complement method where r is the base of the number :

$(3762)_2$ and $(2664)_2$ $(11.0101)_2$ and $(11.100)_2$

(c) State the DeMorgan's theorems.

Minimize the following using K-map technique :

$F(A, B, C, D) = AB'C' + A'BC + A'B'CD + ABCD + \Sigma d(1, 5)$

7. Attempt any **two** parts of the following. All questions carry equal marks :

(a) What are the applications of a CRO ? How do you measure frequency of an unknown signal using Lissajous figure in CRO.

(b) Draw and derive the expression for differentiator with op-amp. What is the range of the voltage gain adjustment in the circuit of Figure 7.

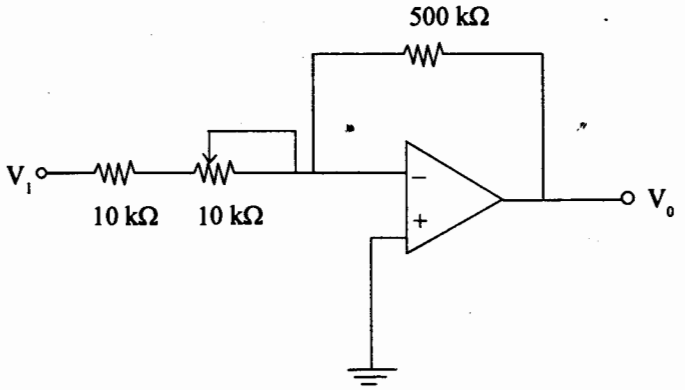

Figure 7